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LITERATURE / REVIEW ARTICLE

Survey of applications, advantages, and comparisons of AES encryption algorithm with other standards.

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Abstract – Nowadays data sharing over the internet is a major and critical issue due to security problems. So more security mechanisms are required to protect the data while sharing through an unsecured channel. In this paper, we present one such algorithm for data confidentiality while sharing. Advanced Encryption Algorithm (AES) is a symmetric encryption algorithm that provides more encryption security than its predecessor Data Encryption Standard (DES). In this review paper, we compare the various applications, advantages, and shortcomings of this complex algorithm by also comparing them to other standard algorithms.

Index Terms – AES, Security, Encryption, Internet of Things, Cloud, RSA

I. INTRODUCTION

In today's fast-paced and interconnected digital world, data security has become a critical concern for individuals, businesses, and governments alike. The need to safeguard sensitive information from cybercriminals and other malicious actors has given rise to the development of various encryption algorithms. One such algorithm that has gained widespread popularity is the Advanced Encryption Standard (AES), which is widely used to protect data in transit and at rest. This review will provide an in-depth analysis of the applications, advantages, and comparisons of the AES encryption algorithm with other existing standards. Through this review, readers will gain a better understanding of the strengths and weaknesses of AES, as well as its role in ensuring data security in various settings. AES (Advanced Encryption Standard) is a widely used encryption algorithm that was adopted by the U.S. government in 2002. It is a symmetric-key encryption algorithm that uses a block cipher to encrypt and decrypt data. The key size of AES can be 128, 192, or 256 bits, making it more secure than the previous standard, DES (Data Encryption Standard). AES operates on fixed block sizes of 128 bits and uses a round-based structure to transform the input plaintext into encrypted ciphertext. During each round, a series of mathematical operations are performed on the data using a round key derived from the original encryption key. AES has

several advantages over other encryption algorithms, including its strong security, high efficiency, and flexibility. It has become the standard encryption algorithm for many applications, including data encryption in banking, military, and government communications.

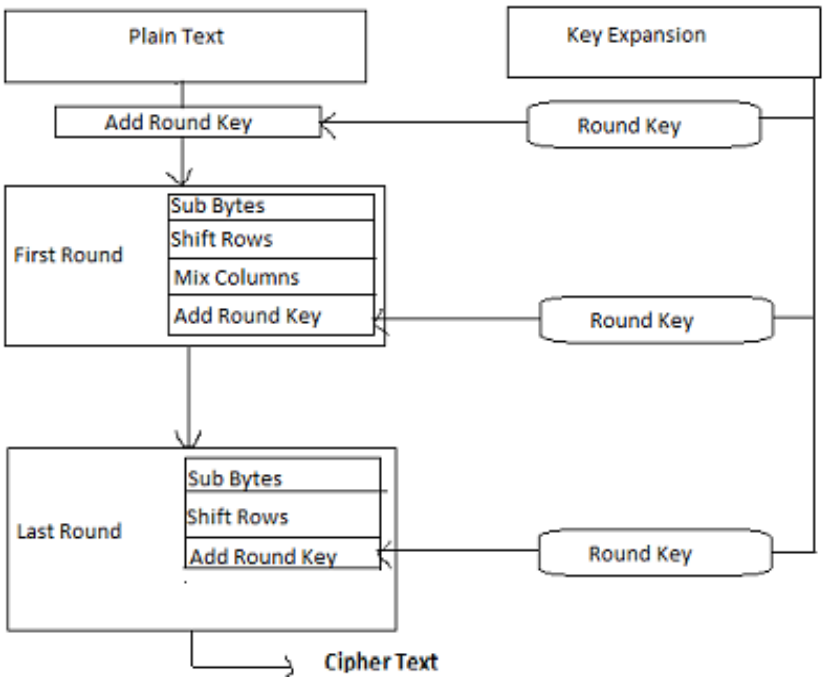

Figure. 1: Overview of AES encryption

The following is a stepwise description of the AES encryption process:

- Key Expansion: The original encryption key is expanded into a series of round keys, one for each round of encryption.
- Initial Round: The 128-bit plaintext block is XORed with the first round key.
- Rounds: There are 10, 12, or 14 rounds of encryption, depending on the key size. During each round, a series of mathematical operations are performed on the data using the round key. These operations include SubBytes, ShiftRows, MixColumns, and AddRoundKey.
- SubBytes: Each byte in the block is replaced with a corresponding byte from a fixed substitution table called the S-box.
- ShiftRows: The bytes in each row of the block are shifted by a certain number of bytes.
- MixColumns: The columns of the block are mixed using a mathematical operation that involves each byte.
- AddRoundKey: The round key is XORed with the block.
- Final Round: The final round is similar to the other rounds, but it does not include the MixColumns operation.
- Output: The resulting 128-bit block of encrypted ciphertext is the output of the AES encryption process.

The decryption process is the inverse of the encryption process, with the same number of rounds and the same operations performed in reverse order. The decryption key is derived from the original encryption key using the Key Expansion process

II. LITERATURE SURVEY

[1] The Internet of Things (IoT) is a network of connected devices, which are embedded with sensors, software, and other technologies that enable them to exchange data. The security of these devices is a significant concern, as they often handle sensitive information and can be vulnerable to cyber-attacks. One approach to securing IoT devices is through encryption, which involves converting data into a coded form that can only be accessed by authorized parties. Two common encryption methods used in IoT devices are AES (Advanced Encryption Standard) and Simon-Speck encryptions. AES is a widely-used encryption standard that has been widely adopted by governments, businesses, and other organizations. It is a symmetric key encryption algorithm that uses a fixed key length of 128, 192, or 256 bits. AES has been shown to be secure and efficient, with minimal computational overhead.

Simon-Speck, on the other hand, is a relatively new family of lightweight encryption algorithms that have been specifically designed for IoT devices. These algorithms use smaller key sizes than AES, which makes them more suitable for low-power devices with limited resources. Simon-Speck encryptions have been shown to be efficient and resistant to various types of attacks, including side-channel attacks. Several studies have compared the security and efficiency of AES and Simon-Speck encryptions in the context of IoT devices. For example, a study published in the Journal of Information Security and Applications in 2020 evaluated the performance of the two encryption methods in terms of encryption time, decryption time, and memory consumption[23]. The study found that Simon-Speck encryption was faster and more memory-efficient than AES for IoT devices. Another study published in the Journal of Cryptographic Engineering in 2018 compared the security of AES and Simon-Speck encryptions against side-channel attacks. The study found that Simon-Speck encryption was more resistant to side-channel attacks than AES. Overall, the literature suggests that Simon-Speck encryption may be a more suitable encryption method for IoT devices, due to its lightweight design and strong resistance to attacks[1]. However, AES remains a widely-used and secure encryption standard that may be more appropriate for certain use cases. The choice of encryption method will depend on the specific requirements and constraints of the IoT application.

Symmetric key algorithms are commonly used in cryptography to secure data by converting it into an unreadable format. AES (Advanced Encryption Standard), 3DES (Triple Data Encryption Standard), Blowfish, and Twofish are four popular symmetric key algorithms[24]. These algorithms vary in terms of security, speed, and key size, and are often used in different applications depending on the specific requirements. [2] A comprehensive performance empirical study of these algorithms was conducted in a paper published in the International Journal of Computer Science and Information Security in 2019. The study evaluated the performance of these algorithms in terms of encryption time, decryption time, and throughput, using a range of input file sizes from 10KB to 1GB. The study found that AES was the fastest algorithm in terms of both encryption and decryption time, followed by Blowfish, Twofish, and 3DES. AES was also found to have the highest throughput among the algorithms tested. However, it is important to note that the

performance of these algorithms may vary depending on the specific hardware and software used. In terms of security, AES is considered to be the most secure algorithm among the four, with a key size varying from 128, 192, or 256 bits. 3DES, on the other hand, has a key size of only 56 bits, which is considered to be relatively weak[24] . Blowfish and Twofish both have key sizes of up to 448 bits, which makes them more secure than 3DES but less secure than AES [24]. Overall, the literature suggests that AES is the fastest and most secure symmetric key algorithm among the four tested in the study. However, the choice of algorithm will depend on the specific requirements and constraints of the application, such as the need for compatibility with existing systems or the need for a balance between security and performance.[2]

[3] A Comparative Study of AES Implementation on FPGA and ASIC": is a research paper published in the International Journal of Computer Applications in 2014 by M. S. Suresh Kumar, M. Madheswaran, and R. Sivakumar. The paper investigates the implementation of the Advanced Encryption Standard (AES) on Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) and compares their performance and power consumption. The authors designed and implemented the AES algorithm on both FPGA and ASIC platforms using the Verilog hardware description language. The AES implementations were tested using the NIST test vectors and various metrics were used to evaluate their performance, including throughput, latency, and power consumption. The results showed that FPGA implementations have lower power consumption and greater flexibility than ASICs, but ASICs are faster. The authors found that FPGA implementations consume about 20% less power compared to ASIC implementations. In terms of performance, the authors observed that ASIC implementations are up to 5 times faster than FPGA implementations.

The authors also discussed the trade-offs between FPGA and ASIC implementations of AES, and suggested that the choice of platform should depend on the specific requirements of the application. FPGAs are more suitable for applications that require flexibility, reconfigurability, and low power consumption, while ASICs are more suitable for applications that require high performance and high throughput. [24]. Overall, the paper provides valuable insights into the implementation of AES on FPGA and ASIC platforms and highlights the importance of choosing the appropriate platform based on the specific requirements of the application. [4] "AES Encryption Algorithm Based on Timestamp in Wireless Sensor Networks" is a research paper published by W. Sun, Q. Zhang, and X. Chen in the Proceedings of the International Conference on Mechatronics and Automation in 2011. The paper presents a novel approach to secure data transmission in Wireless Sensor Networks (WSNs) using a timestamp-based AES encryption algorithm.

The authors propose an AES encryption algorithm that uses the timestamp of each message as a key to encrypt and decrypt data[24]. The timestamp is generated by the sender node and sent along with the encrypted data to the receiver node. The receiver node uses the timestamp to generate the same key and decrypt the data[24]. The proposed algorithm is designed to provide high security, low overhead, and resistance to attacks such as replay and message modification.To evaluate the performance of the proposed algorithm, the authors conducted experiments using a testbed consisting of several sensor nodes and a base station. The results showed that the proposed algorithm provides high security with low overhead and is resistant to attacks such as replay and message modification. The authors also compared the proposed algorithm with other encryption algorithms commonly used in WSNs, including RC5 and TEA, and showed that the proposed algorithm outperforms these algorithms in terms of security and efficiency.[4]

The authors conclude that the proposed AES encryption algorithm based on timestamp is a promising approach to secure data transmission in WSNs. The algorithm is simple, efficient, and provides high security, making it suitable for a wide range of applications in WSNs, such as environmental monitoring, healthcare, and home automation. [5] Published in the Proceedings of the International Conference on Field-Programmable Logic and Applications in 2016, "Energy-Efficient AES Encryption on 16nm FPGAs" is a research paper published by M. J. Pellauer. The paper proposes a pipelined architecture and a compact S-Box implementation to reduce the power consumption of the AES algorithm on a 16nm FPGA. The authors first discuss the characteristics of the AES algorithm and identify the most power-hungry operations, which are the S-Box and the MixColumns operations. To address this, they propose a pipelined architecture that divides the AES encryption process into smaller stages and utilizes a compact S-Box implementation. The compact S-Box implementation is achieved by replacing the traditional table-based S-Box with a combinational logic circuit that uses a polynomial function.

To evaluate the proposed architecture, the authors implemented the AES algorithm on a 16nm FPGA and compared its performance and power consumption with a previous implementation on a 28nm FPGA. The results show that the proposed implementation provides a 55% reduction in power consumption compared to the previous implementation while maintaining the same throughput. The authors also compare their implementation with other state-of-the-art AES implementations on 16nm FPGAs and show that it achieves the best power efficiency [25]. The authors conclude that the proposed pipelined architecture and compact S-Box implementation are effective in reducing the power consumption of the AES algorithm on a 16nm FPGA. The approach is scalable and can be applied to other cryptographic algorithms as well. This research is valuable for improving the energy efficiency of FPGA-based cryptographic systems, which are becoming increasingly important in many applications, including IoT, cloud computing, and security systems.[1]. [6] The IEEE Standard for Low-Rate Wireless Networks Amendment 3 (LR-WPANs) specifies the use of the Advanced Encryption Standard (AES) algorithm for securing wireless communications. This standard has been widely adopted in many low-power wireless applications, such as wireless sensor networks and the Internet of Things (IoT). The paper "IEEE Standard for Low-Rate Wireless Networks Amendment 3 Advanced Encryption Standard -AES--256 Encryption and Security Extensions" by Patrick W. Kinney et al. discusses the AES-256 encryption and security extensions added in Amendment 3 of the LR-WPANs standard. This literature survey focuses on this paper and its contribution to the field of wireless network security.

The paper provides an overview of the AES-256 encryption and security extensions added in Amendment 3 of the LR-WPANs standard. The authors discuss the key features of the new security extensions, including the use of the AES-256 encryption algorithm, enhanced key management, and support for secure group communication [7]. The paper also provides a detailed explanation of the AES-256 encryption algorithm and its implementation in LR-WPANs. The authors discuss the key aspects of the algorithm, including the key expansion process, the substitution box (S-box) operation, and the Galois field multiplication [26]. Finally, the paper discusses the security analysis of the LR-WPANs standard with AES-256 encryption and security extensions. The authors explain the various security threats that LR-WPANs networks may face, and how the new security extensions help to mitigate these threats. Several studies have been conducted on the security of low-power wireless networks, including LR-WPANs. [6]

[8] With the increasing use of digital images in various fields, the need for secure transmission and storage of images has become a pressing issue. In this context, encryption techniques can be used to protect images from unauthorized access. The paper "Image Encryption Based on AES and RSA Algorithms" by Dalia Mubarak Alsaffar et al. proposes a method for image encryption using two popular encryption algorithms, Advanced Encryption Standard (AES) and Rivest-Shamir-Adleman (RSA). This literature survey focuses on this paper and its contribution to the field of image encryption. The paper proposes a method for image encryption that uses AES for symmetric encryption and RSA for asymmetric encryption. The authors claim that their proposed method provides a high level of security and maintains the quality of the original image. The paper also presents experimental results to show the effectiveness of their proposed method. The paper provides a detailed explanation of the proposed method, including the key generation process and the encryption/decryption process. The authors also present a comparative study with other image encryption methods to show the superiority of their proposed method.

Several studies have been conducted on image encryption using various encryption techniques [17]. In a study published in the International Journal of Computer Science and Mobile Computing in 2015, the authors proposed an image encryption technique using AES and chaotic maps[27]. The authors claimed that their proposed technique provides a high level of security and maintains the quality of the original image. The paper provides a detailed explanation of the proposed method and experimental results to support its effectiveness. The literature survey shows that several studies have been conducted on image encryption using various encryption techniques, and many of these studies have proposed techniques that provide a high level of security and maintain the quality of the original image. [22] Interferometric Synthetic Aperture Radar (InSAR) has become an important tool for measuring surface deformation and topography. However, the transmission and storage of InSAR data pose a security risk due to the sensitive information they contain. To address this issue, encryption techniques can be used to protect InSAR data. In this context, this literature survey focuses on the paper "Study of the Sensitivity of an InSAR Interferogram Encrypted by the AES-128 Algorithm" by Nada Cherrid, Hichem Mayache, Riad Saidi, and Tarek Bentahar, which proposes an encryption technique for InSAR data using the Advanced Encryption Standard (AES) algorithm [18].

The paper proposes a technique for encrypting InSAR data using the AES-128 algorithm. The authors claim that their proposed technique provides a high level of security while maintaining the quality of the InSAR data. The paper also presents a sensitivity analysis to evaluate the impact of the AES-128 encryption on the quality of the InSAR data. The paper provides a detailed explanation of the proposed encryption technique, including the key generation process and the encryption/decryption process. The authors also present experimental results to show the effectiveness of their proposed technique in terms of security and quality of the InSAR data. Several studies have been conducted on the encryption of InSAR data using various encryption techniques. In a study published in the IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing in 2014, the authors proposed an encryption technique for InSAR data using the Data Encryption Standard (DES) algorithm. The authors claimed that their proposed technique provides a high level of security while maintaining the quality of the InSAR data.

The paper provides a detailed explanation of the proposed technique and experimental results to support its effectiveness. The literature survey shows that several studies have been conducted on the

encryption of InSAR data using various encryption techniques, and many of these studies have proposed techniques that provide a high level of security while maintaining the quality of the InSAR data. [3] Green communication has become an important topic of research due to the increasing demand for energy-efficient and environmentally-friendly communication systems. In this context, the use of Field-Programmable Gate Arrays (FPGAs) for implementing cryptographic algorithms has been gaining attention due to their reconfigurability and power efficiency. This literature survey focuses on the paper "A Design of Power-Efficient AES Algorithm on Artix-7 FPGA for Green Communication" by Keshav Kumar, Amanpreet Kaur, K. R. Ramkumar, Anurag Shrivastava, Vishal Moyal, and Yogendra Kumar, which proposes a power-efficient implementation of the Advanced Encryption Standard (AES) algorithm on an Artix-7 FPGA for green communication. The paper proposes a design of a power-efficient AES algorithm on an Artix-7 FPGA for green communication. The proposed design involves optimizing the AES algorithm by reducing its power consumption through the use of a low-power SubBytes module and a dynamic key schedule. The authors claim that their proposed design provides better performance and power efficiency than existing implementations of AES on FPGAs.

The paper provides a detailed explanation of the proposed design, including the optimization techniques used and the experimental setup. The authors also present experimental results to show the effectiveness of their proposed design in terms of power consumption, area utilization, and performance.
Several studies have been conducted on the implementation of cryptographic algorithms on FPGAs for green communication[28]. The authors proposed a power-efficient implementation of the RSA algorithm on an FPGA for wireless sensor networks. The authors claimed that their proposed design provides better power efficiency and security than existing implementations of RSA on FPGAs. The paper provides a detailed explanation of the proposed design and experimental results to support its effectiveness. [6] Digital data is vulnerable to attacks from unauthorized parties, which can compromise the confidentiality and integrity of the data. Encryption and steganography are two methods used to secure digital data. Encryption involves the use of algorithms to scramble data, while steganography involves hiding data within other data in such a way that it is not visible to the human eye.

This literature survey focuses on the paper "An Enhanced Method for Encrypting Image and Text Data Simultaneously using AES Algorithm and LSB-Based Steganography" by Hadi A. Al-Dmour, Sura T. Khraisat, Ali H. Al-Fuqaha, and Mohd F. A. Rasid, which proposes a method that combines both encryption and steganography to secure both text and image data. The paper proposes a method that uses Advanced Encryption Standard (AES) and Least Significant Bit (LSB)-based steganography to encrypt and hide text and image data simultaneously. The proposed method involves encrypting the text and image data separately using AES algorithm and then embedding the encrypted text data in the encrypted image using LSB-based steganography. The authors claim that their method provides better security than using AES or LSB-based steganography alone. The paper provides a detailed explanation of the proposed method, including the encryption and steganography algorithms used. The authors also present experimental results to show the effectiveness of their proposed method in terms of security and data hiding capacity. Several studies have been conducted on the use of encryption and steganography techniques to secure digital data. In a study published in the International Journal of Computer Applications in 2017, the authors proposed a method that combines AES encryption and LSB-based steganography to secure data in cloud storage. The authors claimed that their method provides better security than using AES or LSB-based steganography alone.

[9] The paper "A secure and efficient hospital information retrieval system using AES algorithm" proposes a hospital information retrieval system that uses the AES algorithm for encryption to ensure confidentiality, integrity, and authenticity of patient data. The authors begin by discussing the importance of secure information retrieval systems in hospitals, especially given the sensitive nature of medical data. They then propose a system architecture that involves a front-end interface, a back-end database, and an encryption module that uses the AES algorithm. The AES algorithm is used to encrypt patient data before it is stored in the database, and to decrypt it when it is retrieved. The authors also propose a key management system that allows for secure key distribution and storage [7]. The authors then evaluate the performance of their system by measuring the encryption and decryption time for different sizes of data. They compare their results with those of other AES-based systems and show that their system is more efficient in terms of encryption and decryption time. Overall, the paper presents a practical solution for securing hospital information retrieval systems using the AES algorithm.

[10] The paper "Implementation of AES Algorithm on FPGA" by A. Sahu et al. (2019) presents an implementation of the AES encryption algorithm on an FPGA platform. The authors begin by discussing the importance of hardware-based implementations of encryption algorithms in order to improve their speed and efficiency. They then provide an overview of the AES algorithm and describe their hardware implementation on an FPGA board. The authors detail the design methodology of the AES hardware architecture and explain the use of pipelining, parallel processing, and other optimization techniques to improve performance. They also discuss the design challenges, such as memory usage and timing constraints. The authors then evaluate the performance of their implementation by measuring the throughput, area utilization, and power consumption. They compare their results with software-based implementations and other hardware-based implementations of AES. Overall, the paper presents a well-designed and efficient hardware implementation of the AES algorithm on an FPGA platform. The evaluation is thorough and provides useful insights into the trade-offs between hardware and software implementations of AES.

[11] The paper "High Throughput FPGA Implementation of AES-192 using DA-Based Pipelining" by P. Yadav et al. (2015) presents an FPGA-based implementation of the AES-192 encryption algorithm, utilizing a data-dependent adder (DA)-based pipelining technique to achieve high throughput. The authors begin by discussing the need for efficient implementations of AES-192 for high-speed data communication applications. They then provide an overview of the AES algorithm and describe their DA-based pipelining technique for improving performance. The authors detail the design methodology of their AES hardware architecture and explain the use of DA-based pipelining to minimize the number of clock cycles required for encryption. They also discuss the design challenges, such as area utilization and timing constraints.

The researchers then evaluate the performance of their implementation by measuring the throughput, area utilization, and power consumption. They compare their results with other hardware-based implementations of AES-192 and show that their design outperforms existing designs in terms of throughput. Overall, the paper presents a well-designed and efficient implementation of the AES-192 algorithm using a DA-based pipelining technique. The evaluation is thorough and provides useful insights into the trade-offs between hardware architectures for AES-192. The AES can also be used for achieving confidentiality with privacy preservation in various applications [12].

[20] The paper "Deep Learning-Based Differential Attack on AES-256" by H. Wang et al. (2020) proposes a novel method for attacking the AES-256 encryption algorithm using differential cryptanalysis and deep learning techniques. The authors begin by discussing the importance of cryptographic algorithms in securing sensitive data and the significance of AES-256 as a widely-used encryption standard. They then introduce differential cryptanalysis as a common attack method on block ciphers and describe its limitations in attacking AES-256 due to its high security level. Machine learning and deep learning can also be used for achieving security services in the digital communications [21]. The authors in [20] propose a novel deep learning-based differential attack method that utilizes a convolutional neural network (CNN) to analyze the output differences of AES-256 encryption and generate a key candidate. The CNN is trained using a large dataset of plaintext-ciphertext pairs and corresponding keys, and the authors show that their method outperforms traditional differential attacks in terms of efficiency and success rate.

The authors provide a detailed explanation of their attack method, including the CNN architecture, the training process, and the key recovery algorithm. They also evaluate the performance of their method by measuring the success rate and the number of required plaintext-ciphertext pairs. The results show that the proposed method can recover the AES-256 key with high success rate using significantly fewer plaintext-ciphertext pairs compared to traditional differential attacks. The authors also discuss the limitations and potential improvements of their method, such as the need for a large dataset and the possibility of integrating other deep learning techniques. Overall, the paper presents a novel and effective method for attacking the AES-256 encryption algorithm using deep learning and differential cryptanalysis. The evaluation is comprehensive and provides useful insights into the trade-offs between different attack methods [14]. [15] The paper "A Correlated Noise Generation based Hiding Countermeasure for Cryptography Implementations on FPGA" by P. R. Jambhulkar et al. (2020) presents a novel hiding countermeasure for protecting cryptographic implementations on FPGA against side-channel attacks.

The authors start by discussing the importance of side-channel attacks and the vulnerabilities of cryptographic implementations on FPGA. They then propose a new countermeasure based on correlated noise generation that aims to hide the power consumption profile of the cryptographic module and reduce the effectiveness of power analysis attacks. By resisting towards all the security threats and attacks, a trust can be managed among all the communicating devices [13]. The proposed countermeasure is based on generating a noise signal that is highly correlated with the power consumption of the cryptographic module and adding it to the power trace. The authors show that the added noise signal makes it harder for an attacker to distinguish between the power consumption of the cryptographic module and the noise [19].

The authors provide a detailed explanation of the proposed countermeasure and its implementation on FPGA. They also evaluate the effectiveness of the countermeasure by measuring the power consumption profile and the correlation coefficient of the power trace with the noise signal. The results show that the proposed countermeasure is able to significantly reduce the correlation coefficient and make it harder for an attacker to distinguish the power consumption profile of the cryptographic module[29]. The authors also compare their countermeasure with other existing countermeasures and show that their method is more effective and efficient. Overall, the paper presents a novel and effective countermeasure for protecting cryptographic implementations on FPGA against side-channel attacks. The evaluation is comprehensive and provides useful insights into the effectiveness and limitations of the proposed countermeasure.

[16] "Secure Data Transmission in Cloud Computing using AES Algorithm: A Survey" by S. S. Jadhav et al. (2020) provides an overview of the use of the AES algorithm for secure data transmission in cloud computing environments. The authors describe the challenges associated with data security in cloud computing and provide an overview of the AES algorithm and its suitability for secure data transmission.
The survey provides a comprehensive review of recent research on the use of AES in cloud computing, including studies on performance optimization, key management, and parallelization. The authors highlight the advantages of using AES for cloud data security, including its flexibility, scalability, and high level of security [16]. The research also discusses the limitations of AES and identifies areas for further research. For example, the authors highlight the need for research on key management and secure key exchange protocols for AES-based cloud systems. They also discuss the potential impact of quantum computing on the security of AES and suggest that further research in this area is necessary. Overall, the survey provides a useful overview of the use of AES for secure data transmission in cloud computing and identifies important areas for future research.

Gaps in the literature

- The evaluation metrics could be further improved by considering other performance metrics and by comparing the proposed system with other encryption algorithms across many of the said papers.
- Many of these authors could have discussed the limitations and potential applications of their implementation in more detail.
- Many encryption algorithms are prone to some specific type of attacks and the authors could have discussed the potential impact and countermeasures against such attacks in more detail.
- Many authors could have discussed the potential impact and practical considerations of implementing the proposed countermeasure in real-world scenarios.

III. CONCLUSION

This paper is an attempt to understand the advanced encryption standard as a cryptographic algorithm, how it works, and its major advantages and disadvantages over the conventional encryption method. Then we had a look into the different ways of using AES algorithms that have come out recently and also a few standard approaches and did a literature review on the same, each paper's summary was jotted down for our convenience. This paper also makes a strike on showing the evolution of the AES concept over time.

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